What Is Claimed Is:

1. An apparatus for detecting errors in a multiple processor system, comprising:

at least two processors, each processor including a plurality of pipeline stages for processing the same instructions;

wherein each pipeline stage includes a parity bit generator, the parity bit generator generating at least one parity bit for each stage; and

a comparing circuit intercoupled to the processors, the comparing circuit comparing the parity bit of a stage of one processor to the parity bit of the same stage of another processor, and indicating an error when the parity bits are different in value.

2. The apparatus of claim 1, wherein the comparing circuit causes both processors to flush and restart when the parity bits are different in value.

3. The apparatus of claim 1, wherein the comparing circuit indicates an error before an answer is computed by both processors at the completion of the plurality of pipelined stages for both processors.

4. The apparatus of claim 1, wherein the comparing circuit indicates an error in response to a single event upset occurring in at least one processor.

5. The apparatus of claim 1, wherein the comparing circuit indicates an error in response to single bit and double bit errors occurring in the system.

6. A machine-readable medium having stored thereon a plurality of executable instructions, the plurality of instructions comprising instructions to:

process the same instructions for at least two processors;

compare at least one parity bit of a pipeline stage for one processor with at least

one parity bit of the same stage of another processor; and

indicate an error when the parity bits are different in value.

7. The medium of claim 6, wherein said instructions include instructions to flush and restart both processors when the parity bits are different in value.

8. The medium of claim 6, wherein said instructions include instructions to indicate an error before an answer is computed by both processors at the completion of the plurality of pipelined stages for both processors.

9. The medium of claim 6, wherein the difference in parity bit value is caused by a single event upset occurring in at least one processor.

10. The medium of claim 6, wherein said instructions include instructions to indicate an error in response to both single bit and double bit errors occurring in at least one processor.

11. A method for detecting errors in a multiple processor system, comprising:

processing the same instructions during a plurality of pipeline stages for at least two processors;

generating at least one parity bit for each stage;

comparing the parity bit of a stage for one processor with the parity bit of the same stage of another processor; and

indicating an error when the parity bits are different in value.

12. The method of claim 11, further comprising:

flushing and restarting both processors when the parity bits are different in value.

13. The method of claim 11, wherein the step of indicating includes indicating an error before an answer is computed by both processors at the completion of the plurality

of pipeline stages for both processors.

14. The method of claim 11, wherein the step of indicating includes indicating an error in response to a single event upset occurring in at least one processor.

15. The method of claim 11, wherein the step of indicating includes indicating an error in response to both single bit and double bit occurring in the system.